CMC081

Sixteen Channel Charge Integrating ADC

Firmware version 3, October 2005

Cheesecote Mountain CAMAC, 24 Halley Drive, Pomona, NY 10970
tel (845) 364 0211, fax (845) 362 6947, www.cmcamac.com, info@cmcamac.com

CMC081

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General Information

Unpacking and inspection

It is recommended that the shipment be thoroughly inspected immediately upon delivery. All material in the container should be checked against the Packing list and damage or shortages reported promptly.

Warranty

Cheesecote Mountain CAMAC warrants its products to operate within specifications under normal use and service for a period of one year from the date of shipment. Replacement parts and repairs are warranted for a period of one year. This warranty extends only to the original purchaser. In exercising this warranty, CMC will repair, or at its option, replace any product returned to us within the warranty period, provided that our examination discloses that the product is defective due to workmanship or materials and has not been damaged by misuse, neglect, accident or abnormal conditions of operation. The purchaser is responsible for the transportation and insurance charges arising from return of products for service. CMC will return all in-warranty products with transportation prepaid.
This warranty is in lieu of all other warranties, expressed or implied, including but not limited to any implied warranty of merchantability, fitness, or adequacy for any particular purpose or use. CMC shall not be liable for any special, incidental, or consequential damages, whether in contract or otherwise. CMC products are not designed for use in life support situations or in situations where the operation of the device is essential to assuring health or safety.

Service Procedure

Products requiring maintenance should be returned to CMC. The products returned must be labeled with a Return Authorization Number issued by CMC prior to shipment of the product. All products returned for service must be accompanied by information including the description of the problem and the name, phone number and any other contact information for the user who is returning the product
If under warranty, CMC will repair or replace the product at no charge. The purchaser is only responsible for transportation charges for the return of the product to CMC.
For all products in need of repair after the warranty period, the customer must provide a Purchase Order Number before any inoperative equipment can be repaired. The customer will be billed for the parts and labor for the repair as well as for shipping.

Firmware

The CMC203 makes extensive use of programmable logic. Occasionally a bug will be found and corrected, or a feature changed or added to improve performance in particular application. These changes are readily accomplished by modifying the programmable logic that controls the module. Please bring any errors in the operation or behavior of the module to our attention for evaluation and correction. Firmware upgrades, when available, will be made without charge (except shipping) when the module is returned to CMC.

Documentation

CMCAMAC is continually improving the quality and performance of its products. Unfortunately, this process can result in documentation that differs in minor details from the products themselves. Where discrepancies arise please be assured that the unit is correct and incorporates the latest modifications to the design. Please bring any errors or omissions in the documentation to our attention for evaluation and correction.

Contact Information

Questions concerning the installation, calibration and use of this equipment should be directed to Cheesecote Mountain CAMAC, 24 Halley Drive, Pomona, NY 10970, Tel 845 364 0211, fax 845 362 6947. Questions can also be forwarded via Email to info@cmcamac.com. The most current information regarding this product can also be found at www.cmcamac.com

Basic Specifications:

Power up as LeCroy 4300b in 11 bit mode.

50 ohm input impedance
gate width 20ns to 500 ns
Compatible with LeCroy 4300b
Dead time 8.5 microseconds in Fera mode
pedestal memory and subtraction
zero and overflow suppression
Camac commands and status word as in 4300b
all other specifications similar to 4300b, whenever possible.

This basic mode is a substitute for the LeCroy 4300b with similar characteristics. This module is not an exact replacement, there are some differences.

- The FERA readout timing is slightly slower. The CMC081 uses an 80 MHz state machine, rather than hard wired ECL logic, to perform the handshakes. The delay from the end of WAK to the next WST is about 40-50 ns.
- The test pulse supplies a DC level (from the DAC input) to the inputs, not a pulse.
- The random Camac data is not cleared by F9
- The full scale and lsb are smaller, 250 pC and 125 fC instead of 500 pC and 250 fC

CMC081 enhancements and added features:

- Built in sliding scale, final DNL <1%.
- Separate sparse readout thresholds independent of pedestal subtraction.
- Two ranges, 8:1, full scale 2 nC or 250 pC.
- Selectable 11 bit or 12 bit mode for each range.
- Improved Fera readout mode.
- FIFO buffers for both Fera and Camac readout.
- Busy output
- Analog Sum output
- Gate Enable / disable
- Four channel mode (0,4,8,12), with reduced dead time (< 4μs)

Gain*

Low range, 11 bit mode	125 fC lsb	250 pC fs (power up default)
Low range, 12 bit mode	62 fC lsb	250 pC fs
high range, 11 bit mode	1000 fC lsb	2000 pC fs
high range, 12 bit mode	500 fC lsb	2000 pC fs

*with standard input termination-attenuation circuit. Other gains are possible by using a different attenuation.

Camac Commands, function code and subaddress:

Compatible with LeCroy 4300b commands

F0, A0	read status register
F1, A0-15	read pedestal memory
F2, A0-15	read data (random access mode)
F2, A0	read data (sequential access mode)
F8, A0	test LAM
F9, A0	clear module
F10, A0	test and clear LAM
F16, A0	write status register
F17, A0-15	write pedestal memory
F25, A0	generate test event

Unique to CMC081

F0, A1	read cmco081 status register
F0, A2	read sliding scale dac register
F0, A3	read firmware version number, read only
F0, A4	read test gate width, 8 bits, lsb 50 nS, default 3
F0, A5	read request delay register, 10 bits, lsb 50 nS, default 167
F3, A0-15	read raw low range, 14 bits
F4, A0-1	read raw high range, 14 bits
F6, A0-15	read pedestal for high range
F7, A0-15	read threshold registers
F16, A1	write cmc081 status register
F16, A2	write sliding scale dac register
F16, A4	write test gate width register
F16, A5	write request delay register
F22, A0-15	write high range pedestal registers
F23, A0-15	write threshold registers
F24, A0	disable gate
F24, A1	disable gate
F26, A0	enable gate, respect inhibit (default on power up)
F26, A1	enable gate, ignore inhibit

F30	enter programming mode

The following instructions are only available in programming mode

F29	select flash memory mode
F28*	select Camac programming mode
F25	send program pulse
F21	select alternate program
F17*	write to flash memory
F16*	write directly to fpga
F14	test INIT signal from fpga
F13	test DONE flag from fpga
F12	test RDY line from fpga
F6*	read from flash memory (requires readdee program in fpga)
F9	return to normal mode, disable all programming comands

* these instructions are used only during reprogramming of the flash memory, and are not normally required

Status Registers

F16, A0, F0, A0 LeCroy 4300b control register

bits 0-7 virtual station number, this appears in the ls 8 bits of the header when Fera compressed readout is selected.
bit 8 subtract pedestals when Fera readout is selected
bit 9 compress data for Fera readout, the data after pedestal subtraction must be greater than zero, or the channel will be suppressed.
bit 10 Select Fera readout (0= Camac readout). The 4300b has no provision for both.
bit 11 subtract pedestals when Camac readout is selected
bit 12 compress data for Camac sequential readout
bit 13 select Camac sequential readout instead of random Camac readout.
bit 14 enable LAM, LAM is asserted at end of event.
bit 15 suppress overflows in compressed modes.

This register defaults to FF00h on power up or Camac Z.

F16, A1, F0, A1, CMC081 control register

Bit 0 1= enable Fera blocking mode. The 4300b will pass REN while it is busy converting, but before it raises REQ. This mode does not pass REN when busy, and just waits until conversion is finished and REQ is asserted.
Bit 1 0= 11 bit mode, 1= 12 bit mode. This increases the resolution. The full scale is unchanged, only the number of ADC bits used changes.
Bit 2 not used
Bit 3 0= low range, 1= high range. This selects either of the two ranges in the MIQ401 to be digitized. The other range is not digitized.
Bit 4 0= single range, 1= both ranges. This forces both ranges to be digitized. The dead time is longer as a result.
Bit 5 disable sliding scale. This is simply a diagnostic, used during test and to adjust the sliding scale gain.
Bit 6 not used
Bit 7 automatic clear (ECLbus clear not required). This ends busy when digitizing and processing are complete, and does not wait for an ecl clear.

Other Registers

F16, A2, F0 A2 Sliding Scale Dac

This 8 bit register is the value sent to the sliding scale 8 bit DAC. The DAC output is input to one side of the differential input to the ADC. The digital value is always added to the output of the ADC. When the sliding scale is enabled, the DAC value is incremented at the end of each event.

F0 A3 Firmware Version Number

This read only register is simply a version number for the FPGA code.

F16, A4, F0 A4 Test Gate Width

This 8 bit register determines the width of the gate produced by F25, A0. The lsb is 50 ns, and the default value is 3, or 150 ns.

F16, A5, F0 A5 Request Delay

This 10 bit register sets the minimum delay between the end of the gate and the assertion of REQ (when in Fera mode). The delay is 50 ns times the value, plus about 150 ns. If the delay is set less than the actual conversion time, REQ will be asserted promptly at the end of conversion. The maximum delay is about 50 microseconds.

F17, A0-15, F1 A0-15 Pedestal Memory For Low Range

These are the 16 values to be subtracted from the low range ADC values when pedestal subtraction is enabled. This register is compatible with the LRS4300b.

F22, A0-15, F6 A0-15 Pedestal Memory For High Range

These are the 16 values to be subtracted from the high range ADC values when pedestal subtraction is enabled and high range is selected. This register is unique to the CMC081.

F23, A0-15, F7 A0-15 Threshold For Compression Modes

These are the 16 values to be compared with the (possibly pedestal subtracted) ADC values when data compression is enabled. This register is unique to the CMC081. When these registers are set to zero (the default), the compression modes behave as the LRS4300b.

Other Commands

F8, A0, Test LAM
This returns Q = 1 if the LAM is asserted.

F9, A0, Clear Module
This clears the data in the fifo buffers and resets the module. It does not clear any registers.

F10, A0, Test and Clear LAM
Tests the LAM, as F8, and also clears the LAM if it was asserted.

F24, A0, Disable Gate detection, both enable modes

F24, A1, Disable Gate detection, both enable modes

F25, A0, Generate Test Gate
This produces a Gate which is OR'ed with the gate from the Fera control bus. The width is controlled by the register at F16, A4. This Gate will integrate the DC signal due to the dac voltage from the Fera control bus. The conversion factor is 100 microamps per volt. For example, 10 volts at the dac input and a 500 ns gate length produces a 500 pC signal in the MIQ.

F26, A0, Enable Gate detection with inhibit
This enable respects Camac Inhibit. If Inhibit is asserted, the module is disabled. This enable is asserted at power up.

F26, A1, Enable Gate detection
This enable ignores Camac Inhibit.

Data Read Commands

F2, A0-15 Random Camac Read
If sequential Camac readout is disabled, these are the processed values for the 16 channels.

F2, A0 Sequential Camac Read
If sequential Camac readout is enabled, these are the processed values for the 16 channels in order, with Q= 1 until all values have been read. This data comes from the Camac fifo buffer, and cannot be reread..

F3, A0-15 Random Camac Read, Raw Low Range
This is the raw 14 bit ADC value for the low range, without pedestal subtraction

F4, A0-15 Random Camac Read, Raw High Range
This is the raw 14 bit ADC value for the high range, without pedestal subtraction

The Front Panel

Top to Bottom

LEDs

N	lights when module is addressed
A	lights when module is enabled
B	lights when module is Busy

Fera Ecl control bus connector, 8 pair, differential ecl

pair	
1	Not used, connected to ground
2	WST output
3	REQ output
4	CLR input
5	GATE input
6	WAK input
7	GND connected to ground
8	DAC input, 0-10.23 volts (analog)

Behind and between these two connectors is the termination LED. When lighted, it indicates that at least one of the pull down resistor sips is installed.

Fera auxiliary signal connector, 5 pair, differential ecl

Pair	
1	REN input
2	PASS output
3	BUSY output. The BUSY output can be used to control the trigger. It begins at the leading edge of the gate, and ends when the module is cleared (e.g., when an Eclbus CLR is received).
4	ASUM analog sum of all channels on pin 7, pin 8 grounded. The ASUM output can be used in a secondary trigger, or as a monitor. This is an AC coupled, negative signal, the sum of 10% of each input signal
5	Not used, not connected

Signal input Connector, 17 pair, Zin 50 Ohms

Pairs 1-16 Channel 0-15

Pair 17 not used, pins 33 and 34 are connected to ground through 976 Ohm resistors

FeraBus Output Connector, 17 pair, differential ecl

Pairs 1-16 Fera Bus

Pair 17 not used, pins 33 and 34 are connected to ground through 976 Ohm resistors

Note: Differential ecl signals have the odd numbered pin positive true.

Operating Instructions

At Power up, the CMC081 behaves like a LeCroy 4300b Fera ADC.

The 4300b control register is set to FF00h, exactly as the LeCroy module.
The CMC081 control register is set to zero.
The module is enabled and Inhibit is obeyed.

The GATE signal must precede the input signal by at least 25 ns, just as the LeCroy 4300b and 1885 adc modules. The GATE is delayed internally by 20 ns before being applied to the MIQ401s. Input signals should be inside the delayed GATE by at least 5 ns, and end before the end of the delayed GATE.

For Fera readout, The FERA control bus and FERA data bus are connected to the Fera driver. The last module on the bus should have the pull down and termination resistors installed. These are the light blue resistor packs (sips, total of 7) in sockets, and can be accessed by removing the top cover. All other modules should have these resistor sips removed. Note that the 8 pin sips are symmetric and can be installed either way. The 10 pin sips are not, and must be installed correctly.

The REN input and PASS outputs are connected in the daisy chain from REO on the Fera driver.

Input signals are terminated in 50 Ohms and clamped at +0.7 volts and –3 volts.

For Camac readout (without a Fera driver), only the input signals and the GATE are required.

Buffered Readout modes

The sequential Camac readout is buffered with a 255 word deep fifo. If autoclear is enabled, BUSY ends at the end of conversion, and does not wait for an ecl CLR on the control bus. The Camac readout then can occur as a background task. The BUSY will remain on at the end of conversion if there is not enough room in the fifo for another event.

The Fera readout is also buffered with a 255 word deep fifo. If autoclear is enabled, BUSY ends at the end of conversion, and does not wait for an ecl CLR on the control bus. As in the Camac case, the BUSY will remain on at the end of conversion if there is not enough room in the fifo for another event.

High Speed Four channel Mode.

The CMC081 contains 2 complete programs for the fpga in its' flash memory. The normal program, described above) is loaded on power up. The alternate program is selected with a short sequence of ordinary Camac instructions. Reprogramming the fpga takes about 500 mS.

This mode digitizes only 4 of the 16 channels, one from each of the 4 MIQ401 chips. The 16 channels are digitized in the sequence 0,4,8,12,1,5,9,13,2,6,10,14,3,7,11,15. This requires 4 passes through the MIQ chips. The 4 channel mode makes only one pass , digitizing only 0,4,8 and 12. The dead time in this mode is between 3 and 4 μs, depending on the readout mode. For example, in uncompressed FERA mode, the REQ line is asserted after 3.5 Us.

Selecting the Four channel mode

All of the sequencing and control logic is implemented in the Xilinx Spartan II FPGA. The FPGA is RAM based, and must be reloaded each time that power is applied. This is normally transparent to the user, and a few hundred milliseconds after power is applied, the FPGA is ready to use.
The flash memory is large enough to store two complete programs for the FPGA, the normal program, and an alternate program. To load the alternate program, follow this sequence of CAMAC instructions.

F30 this enables the FPGA programming mode, with the normal program selected. The FPGA is cleared and a limited set of CAMAC commands are available.
F21 this selects the alternate program, omit this step to reload the normal program
F25 begin programming from the selected part of the EEPROM
F14 test FPGA INIT line, Loop on this command until Q = 1
F13 test FPGA DONE line. Loop on this command until Q = 1
F9 Exit programming mode

To return to the normal, 4300 compatible mode, either cycle the power, or repeat the above instruction sequence, omitting the F21 command.

Data Formats

Fera outputs

Header for compressed mode
Bits
0-7 VSN from 4300 control register
8-10 not used, 0
11-14 word count, the number of data words following, 0= 16 words
always = 1, indicates header word

Compressed mode, 11 bit mode
bits
0-10 ADC data, pedestal subtracted
11.14 channel number
15 always 0

Compressed mode, 12 bit mode
bits
0-10 ls 11 bits of 12 bit ADC value, pedestal subtracted. Full scale is halved
11-14 channels number
15 always 0

Uncompressed mode, 11 bit mode
bits
0-10 ADC data, pedestal subtracted
always 0

Uncompressed mode, 12 bit mode
bits
0-11 ADC data, pedestal subtracted
12-15 always 0

Camac Sequential outputs. These are 24 bit words.

Compressed mode, 11 bit mode

bits	
0-10	ADC data, pedestal subtracted
11-14	channel number
15	always 0
16-19	channel address
20-23	always 0

Compressed mode, 12 bit mode

bits	
0-10	ls 11 bits of 12 bit ADC value, pedestal subtracted. Full scale is halved
11-14	channel number
15	always 0
16-19	channel address
20-23	always 0

Uncompressed mode, 11 bit mode

bits	
0-10	ADC data, pedestal subtracted
11-15	always 0
16-19	channel address
20-23	always 0

Uncompressed mode, 12 bit mode

bits	
0-11	ADC data, pedestal subtracted
12-15	always 0
16-19	channel address
20-23	always 0

Camac Random outputs. These are 24 bit words.

Using F2, 11 bit mode

Bits	
0-10	ADC data, pedestal subtracted
11-15	always 0
16-19	channel
20	range indicator
21	always 0
22	overflow indicator
23	over threshold indicator

Using F2, 12 bit mode

Bits	
0-11	ADC data, pedestal subtracted
12-15	always 0
16-19	channel
20	range indicator
21	always 0
22	overflow indicator
23	over threshold indicator

Using F3 or F4, Raw ADC data

Bits	
0-13	ADC data
14	ADC out of range indicator
15	0
16-19	channel
20	range indicator
21	always 0
22	overflow indicator
23	over threshold indicator

The Internal Details Of The CMC081

The underlying technology of this module is the LeCroy MIQ401 four channel charge multiplexer. This chip was used as the basis of the LeCroy 1885 FASTBUS ADC and the LeCroy 1182 VME ADC. For the CMC081, these have been packaged in a modern 28 pin soic (small outline integrated circuit) package.

The MIQ401 provides two ranges by internally splitting the signal into 3 parts, in the ratio 8:1:1. The largest split (80% of the input current) is integrated as the low range, one of the 10% splits is used for the high range and the last 10% is used for the analog output (active only during the gate).

The full scale of each integrator is 180 pC. This corresponds to 1440 pC on the high range. The termination circuit at the input shunts 13% of the signal, sending 87% to the MIQ401. The full scale measured at the input is 250 pC and 2000 pC. For the 11 bit mode on the low range,this corresponds to an lsb of 125 fC, (62 fC for 12 bit mode).

The gain can be made identical to the LeCroy 4300b by changing 2 resistors at the input to each channel. The 57.6 ohms is replaced with 88.7 ohms and the 392 ohms is replaced with 113 ohms. These are 0805 size surface mount resistors and with proper tools, they are easily changed. This change will double the lsb and fs for both ranges and resolutions, and will increase the effective noise. The CMC080 can be ordered with either setup. The module will normally be supplied with the higher gain (256 pC fs, 125 or 62 fC lsb).

Each of the 4 MIQ401 chips is supplied with op amp integrators and level shifters for both high and low ranges. The 8 final signals (high and low for each of the 4 MIQs) are multiplexed into a fast 14 bit ADC (only the 11 or 12 msb are used, except for the raw readout). Readout of the 4 MIQ chips is interleaved, with the channel readout sequence of 0,4,8,12,1,5, … 11,15. This results in a total readout time of 4 us for single range mode.

The control logic, registers and data memory buffers are all in the Xilinx Spartan2 fpga. The fpga configuration data is stored in a 4Mb flash memory, which is in a socket. Firmware upgrades (and bug fixes!) are easily accomplished by replacing the flash memory chip.

The GATE signal is edge detected. The enable signal allows detection of the leading edge, which, in turn, enables detection of the trailing edge. This avoids GATE clipping when the module is being enabled or disabled. The MIQs are normally held in reset, to ensure a consistent initial condition. The reset is turned off during the 20 ns GATE delay.

Removing the Pull Down and Termination Resistors

When the CMC081 is used in a FERA system with more than one module, the termination and pull down resistors must be removed from all but one of the data modules. Normally, only the module furthest from the FERA driver retains these resistors.

To remove or replace these resistors, the top cover must be removed. A small (1/4”) open end wrench is helpful to keep the hex standoff from turning. The screws are all 4-40 flat head. To remove both covers, remove the screws from the bottom side (right side when viewed from the front panel), leaving the top side intact. The standoffs will remain attached to the top cover. To remove only the top, remove only the screws in the top cover. The standoffs will stay on the module.

Schematics