CMC202 CAMAC Variable Delay

Two channels in a single width CAMAC module

Each channel:

Input OR, one NIM, one differential ECL
Auxiliary input, differential ECL
Output Fanout, one pair complementary NIM, three differential ECL

CAMAC Six bit delay selection, 0 to 31.5 nS, in 0.5 nS steps:
Delay setting F16, read by F0, A0, A1 selects channel
Delay increment F25(A0,A1), or Auxiliary input, increases by 0.5 nS

Delay accuracy ± 250 pS (can be trimmed for improved accuracy)
Bandwidth > 500 MHz (ECL-ECL)
Delay is provided by differential twisted pair delay lines using high speed differential ECLiPS logic gates.
Insertion delay, ECL-ECL 9 ns, NIM-NIM 11 ns.
Delay stability better than ±100 pS over normal temperature range (to be verified)

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