CMC203 FERA Driver/Memory/Histogrammer

This module can replace the LeCroy 4301 or LeCroy 4301-4302, and 4301-histogrammer combinations. This is a compatible upgrade, not an identical replacement

ALL 4301 CONNECTORS:

- FERA data bus input (34 pin header, single ended ECL)
- FERA control bus (8 ECL)
- CLEAR input Lemo & ECL
- GATE input Lemo & ECL
- IRI input Lemo & ECL
- WAK input Lemo & ECL for FERA output
- WSO output Lemo & ECL write strobe for FERA output
- RQO output Lemo & ECL readout enable & request for FERA output
- REO output ECL readout enable (with inhibit)
- FERA data bus output (34 pin header, differential ECL)

12 bit DAC as in 4301, output 0 to 10.23 Volts
Emulates LeCroy 4301 on power up.

NEW FEATURES
Additional Connector: PSI input, ECL, pass from last module
Optional Time Outs to prevent FERA system hangs
Test GATE output, width set by CAMAC register.
Optional BUSY outputs for trigger control.
 compliant
New Operating Modes:

- Buffered 4301, 2k FIFO buffer between FERA in and FERA out.
- Buffer Mode:1M 16 bit words. Written from FERA input data, read by CAMAC. Can write and read simultaneously.
- Histogram Modes:Thirty two Histograms, 16 bits wide, 15 bit address. Can histogram (separately) all modules in a crate (i.e., 352 channels of 4300b, each in a separate histogram), or make 32 successive histograms a single module (time dependent spectra). Optional 32 bits wide (double word), half of as many histograms.
- LeCroy 3377 TDC Ping Pong Mode: Provide alternate stop pulses to two FERA TDCs, read FERA data into 1M word FIFO buffer for unlimited time range TDC

OPERATION:

- Behavior defaults to 4301 emulation on power up
- Other modes selected by CAMAC instructions
- CAMAC instructions compatible with LeCroy 4301.
- Memory can be read with *FAST*CAMAC, level 1 & 2, up to 20 Mbytes/sec

MECHANICAL

- Single width CAMAC, FERA data bus output connector on rear panel
- Use the CMC204 FERA Mixer to move the FERA output to the front of the crate, or to combine FERA data streams

Cheesecote Mountain CAMAC, 24 Halley Drive, Pomona, NY 10970
tel (845) 364 0211, fax (877) 840 0023, www.cmcamac.com, info@cmcamac.com

The CMC203 has five basic modes of operation

- As a plain 4301 FERA driver. ECL in and ECL out, no buffering. This mode is a drop in replacement for a LeCroy 4301 and is the default mode on power up. All other modes are selected using CAMAC commands

- As an enhanced 4301, ECL in and ECL out. With a 2k FIFO buffer, input and output handshakes (wst/wak) are independent and de-coupled. This works well with a simple memory module as the destination.

- As an enhanced 4301, ECL in and ECL out. With a 2k FIFO buffer and the addition of an external ren/pass. This allows another FERA driver to be the data destination, and allows concatenation of multiple FERA data streams.

- As a FERA driver and memory combination. ECL in and CAMAC dataway readout, with a 1 Mword (1,048,576) FIFO buffer between FERA in and CAMAC out. CAMAC read and FERA input can proceed simultaneously.

- As a FERA driver and histogram memory combination. ECL in and CAMAC readout of the histogram array. The 1 Mword memory is used for histogram storage.

The following features are available in all modes, even the plain 4301 mode. All adjustments and selections are made with CAMAC registers:

12 bit DAC output, 0 to 10.2375 Volts, □1/2 lsb over full range.
The FERA request delay is adjustable from 400 nS to 160 microseconds, in 40 nS steps
Optional pass input to close ren/pass loop
Optional send Clear pulse, width adjustable up to 160 microseconds, 40 nS steps,
Optional send GATE pulse, width adjustable up to 40 microseconds, 10 nS steps
Optional BUSY output (from gate or request input to end of event)
Optional gate timeout, if gate but no request, adjustable up to 160 microseconds
Optional event timeout, if request, but no end of event, adjustable up to to 2.4 milliseconds
Optional clear after event readout
Optional delay after clear before end of event (end of BUSY)
Seven 48 bit counters for gates, requests, clears, headers, timeouts and histogram count.

In the FIFO (list) modes, special headers can be inserted in the data stream when gates, requests, clears or time outs occur. The time of arrival of the GATE leading edge may be inserted in the data stream. In the 1Mword FIFO mode, a Lam is set when the FIFO becomes half full.

In the histogram mode, there is a choice of 16 bit (65k max) or 32 bit (4G max) histogram elements, with corresponding 20 bit or 19 bit address space. The vsn from the header can be concatenated with the data to histogram many modules at once, or a register can be used to select the histogram base address, allowing multiple, time dependent histograms of a 15 bit address space. The readout block size is set by a register to ease readout of histograms with less than 15 bit address spaces. A 48 bit counter records the total number of hits contained in the histogram(s).

FASTCAMAC level 1 readout (400 nS/word) is available in FIFO memory and histogram modes. The module is ready for level 2, requiring only a firmware upgrade when level 2 crate controllers become available.