CMC206 Universal Logic Module

This is a simple module, consisting of a Xilinx XC3S1500-4 FPGA, 4 MegaBytes of fast static ram memory, 54 user i/o connectors, and a complete Camac interface. The Camac interface allows both normal Camac and all levels of FastCamac. The FPGA can be programmed over the Camac interface, or from a pair of flash memory chips (in sockets). The program in flash memory will automatically program the FPGA on power up, or the FPGA can be reloaded by a Camac command.

The Xilinx XC3s1500 FPGA contains about 1.5 Million gate equivalents. In addition to more than 3300 CLBs (each with 4 look up tables and 4 flipflops), there are 32 fast (5 ns) multipliers (for DSP applications), frequency synthesizers and 576k bits of very fast (2.4 ns) block memory.

Sequential logic can be implemented as pipelines, high speed state machines, or as a program in an embedded RISC computer. Internal clocks up to 300 Mhz allow timing applications with precision of a few nanoseconds.

FPGA programs can be written with Xilinx's free Webpack software, the low cost version of their ISE programming package, or other third party software packages

This module can be programmed to provide almost any digital data collection or processing requirement, from simple counters to complex trigger logic or digital signal processing. It can emulate the function of any of the LeCroy ECLine trigger logic modules, at comparable or better speeds, or can add complex trigger processing or real time data analysis to your FERA data stream.

Signal inputs and outputs:

47 differential ECL pairs, arranged in four 0.100” spacing IDC headers
- 34 pin header, 17 pair, on rear panel (A)
- 34 pin header, 17 pair , on front panel (B)
- 16 pin header, 8 pair, on front panel (C)
- 10 pin header, 5 pair, on front panel (C)

7 Nim Fast signals
- 7 Lemo Coaxial connectors, on front panel (N)

The 47 ECL i/o signals can be either input or output, selected by a direction bit, 0 = output, 1 = input. The direction bit controls a DPDT fet switch located between the connector and the ECL driver and receiver. When output is selected, the signal is a differential ECL output with 390 ohm pull down resistors. When input direction is selected the incoming differential signal is terminated in 121 ohms and is connected to the ECL receiver. There are 3 pins (in, out and direction) on the FPGA for each ECL signal, so the choice of input or output is independent for each signal. When output direction is selected, the input pin is not used and vice versa. Some of the termination and pull down resistors are in sockets, to allow the module to be programmed as a FERA compatible data module.

The 7 NIM signals each have only 2 pins on the FPGA. No direction signal is needed, both the input and output signals are always connected to the pin. There is a 50 ohm termination to ground at the connector.

The fast static ram memory consists of four 512k x 16 chips (ISSI IS61LV51216), organized as 1M x 32., two banks of 512k x 32. The most significant address bit must be used as the chip enable (CE0, CE1) to select the bank. The WE and OE are connected to all 4 chips

Programming the CMC206

On power up, the Xilinx XC3s1500 is blank, and must be programmed to be useful. The two 512k flash memory chips supplied with the module contain a simple program to turn the CMC206 into a versatile set of input-output registers. This program is loaded automatically when power is applied.

Programs can be created as schematics, using logic elements (such as gates, flipflops, registers, etc.) or as programs written in VHDL or Verilog. The Xilinx software converts either of these into the programming instructions for the FPGA. This can be loaded directly into the FPGA using Camac instructions, or can be loaded into the flash memory chips to be loaded automatically.

The choice of schematic entry or VHDL is up to the user, either will work correctly. However, we prefer VHDL for complex designs. The examples supplied are written in VHDL, and were compiled using Xilinx ISE 8 software.

Power Requirements:

This module uses both the normal and supplementary 6 Volt pins, both plus and minus. The module cannot be used in a crate that does not support the supplementary power.