A Sliding Scale Method to Reduce the Differential Non Linearity of A Time Digitizer

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Abstract

A novel technique for improving the differential non-linearity (DNL) of an existing time digitizer is presented. Modern subnanosecond time to digital converters that interpolate within a slower clock to achieve a high effective clock rate (and correspondingly small least count) usually exhibit DNL, which is a direct result of imperfections in the interpolation. This can be substantially reduced by applying a sliding scale in the time domain. A comparison of results with and without the sliding scale are presented for a widely used commercial time digitizer.

I. INTRODUCTION

Many application of time digitizers are insensitive to the differential non linearity (DNL). Particle position measurements in a magnetic field use drift chambers and time digitizers (tdc). A histogram of the time of each individual wire may exhibit substantial DNL, often greater than 10%. But the resulting calculated physical quantity (momentum, for example) is the result of a fit to many individual measurements and can have a very small DNL. However, there are many applications that are strongly affected by the DNL. A time of flight spectrometer, which uses only one time digitizer channel, will display the DNL in the final spectrum. A simple ADC can be made by using a time over threshold discriminator and measuring the pulse width with a tdc. However, any DNL in the tdc shows up directly in the histogram.

II. INTERPOLATING TDCS

Most modern time digitizer integrated circuits have a resolution less than 1 nanosecond. This is not accomplished with a multi-gigahertz clock, but by interpolating within a much slower clock period.

This can be done with an analog technique. When a signal arrives, the time to the next from the next clock edge is converted to an analog voltage (for example, by integrating a current, or sampling a ramp waveform), and measuring the voltage with an adc. This can achieve the best time resolution, at the expense of substantial dead time and therefore poor double pulse resolution. To achieve the shortest possible dead time, digital interpolation is usually used.

One of the simplest digital interpolation methods sends the clock waveform down a tapped delay line, and latches the tap outputs when a signal arrives, as shown in figure 1. The time between taps is the resolution. This interpolation method is used in the LeCroy MTD133b integrated circuit [1,2,3]. A 250 MHz (4 nanosecond period) clock is interpolated by 8 to produce a 500 picosecond lsb. The clock is sent down a 2 nanosecond delay line, with taps every 500 picoseconds. The delay line is a series of variable delay CMOS gates controlled by a delay locked loop. The 3 taps are combined to produce a 2 bit grey code, as shown in Table 1. This and a free running grey code counter (counting the 250 MHz clock on both edges, effectively counting at 500 MHz) are combined to produce a grey code counter changing at a 2 GHz rate. The MTD133b has a common input (for start or stop) and 8 signal inputs. The common input latches the grey code into a register, to be used later. The signal inputs latch the grey code into a LIFO memory. During readout, the difference between the common time and the signal time is calculated and output as the time data.

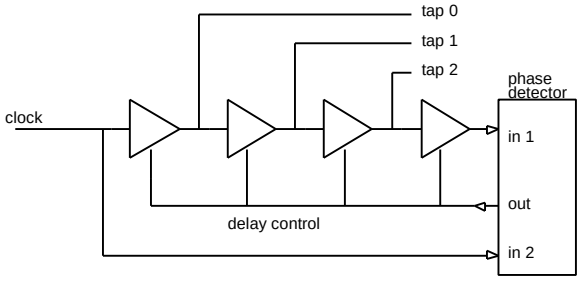

Figure 1. Tapped delay line interpolator and delay locked loop. This is used in the MTD133b to interpolate the 250 MHz clock by eight, producing an effective clock rate of 2 GHz.

Table 1
Digital outputs of the simple interpolator

state	Clock	taps			Grey code output
		t0	t1	t2	
0	0	0	0	0	00
					Counter changes here
1	1	0	0	0	00
2	1	1	0	0	01
3	1	1	1	0	11
4	1	1	1	1	10
					Counter changes here
5	0	1	1	1	10
6	0	0	1	1	11
7	0	0	0	1	01

This interpolation scheme has several sources of DNL. The alignment (the relative delay) of the interpolator and the counter outputs depends on process delays. If this alignment is not perfect, it produces a difference between the 0 and 1 states and also between the 3 and 4 states of the interpolation (these are when one of the bits in the grey counter changes and the

interpolator grey code is stable). If the clock symmetry is not precisely 50/50, counting the clock on both edges produces a difference in the DNL at these two places. Any error in the phase detector that causes the delay line not to be exactly 2 ns long produces DNL similar to the clock asymmetry. If the variable delay line elements are not perfectly matched, or if the delay is different for rising and falling edges, DNL can appear at any place in the interpolation. These DNL sources are confined to the interpolator, and repeat every 8 lsb (the clock period). Finally, since a different bit in the grey counter changes each time (only 1 bit changes at a time) any difference in the propagation delay to each of the 9 latches (common and 8 signal) can also produce DNL. This DNL repeats with the period of the counter, in this case 65,536 lsb.

This raw DNL has no particular symmetry and there can be large errors (a large fraction of an lsb) in any single time measurement. However when the common time is subtracted from the signal time, the DNL of interest is that of the difference. If the DNL is the same for the common and signal (differences will be due only to propagation differences to the different latches, with careful layout, this is very small) the difference DNL is symmetric (This is the DNL of the output of the MTD133b). The measured times are correct, in that averaging multiple measurements will converge on the correct time. However, the width of the time bins will not be the equal, and a smooth spectrum will clearly exhibit this DNL.

Note that DNL due to the different grey code bits of the counter will not be the same, since it depends on the state of the counter, which is different for the common and signal. However, since the counter is free running, multiple measurements average over all counter states (unless the measurements are repeated at exactly the period of the counter), and this source of DNL effectively disappears (it increases the resolution, but does not produce DNL).

There are several interpolating TDC integrated circuits in use at various detectors and laboratories. Most of these suffer (to varying degrees) from the same DNL errors as discussed above.

III. The Sliding Scale

Fortunately the repetitive nature of the DNL of an interpolating tdc makes it relatively easy to eliminate. This can be filtered out in the frequency domain (after data acquisition) or removed with a delay line sliding scale (during acquisition). The sliding scale is a time domain analogue of the traditional sliding scale used in precision adc systems, in which a variable (in steps of the adc lsb) amplitude is added to the input analog signal, and digitally subtracted after the measurement. The DNL is reduced by averaging measurements made using different parts of the adc transfer curve.

In the time domain we can use a variable delay line to change the time of the common signal to the tdc. The time delay is varied in increments of the lsb of the tdc, over a range at least as large as the clock period of the tdc (the clock which is being interpolated). For each measurement, the value of the variable time delay is added to (common start) or subtracted from (common stop) the measurement produced by the tdc. The variable delay is changed after each measurement (or at some regular interval). Each element in a time spectrum is averaged over many neighboring points in the tdc transfer curve, instead of depending on only one point.

Note that errors in the variable time delay will broaden the TDC resolution (the rms noise) in the time domain, just as errors in the added amplitude produce noise in the analog domain. To minimize this, delay errors should be much less than the lsb.

A typical MTD133b will exhibit DNL of several percent, occasionally as high as 10%. This simple sliding scale technique can reduce the DNL to less than 1% , allowing this tdc to be used for many applications previously excluded because of the poor DNL.

IV. Measurements

This technique was tested using a radioactive source (Na^{22}), a small Sodium Iodide crystal and a photomultiplier tube (pmt). The rate was adjusted to be about 30 KHz. This was used both as a random time pulse source and as a random amplitude signal to be measured. A LeCroy 3377 CAMAC TDC provided the MTD133b and a CMC203 [4] CAMAC delay box provided the variable delay (0.5 ns steps from 0 to 31.5 ns). This delay box uses ECL gates to switch twisted pair delay lines, and is adjusted by CAMAC commands.

The random time spectrum was measured with the pmt pulse as a 3377 signal input and a pulse generator as a common stop signal. Figure 2a is the histogram of the raw time spectrum of the TDC. The DNL is about 5% peak to peak and shows a strong repetitive structure. This is a typical MTD133 result. Figure 2b is the same spectrum with the sliding scale.

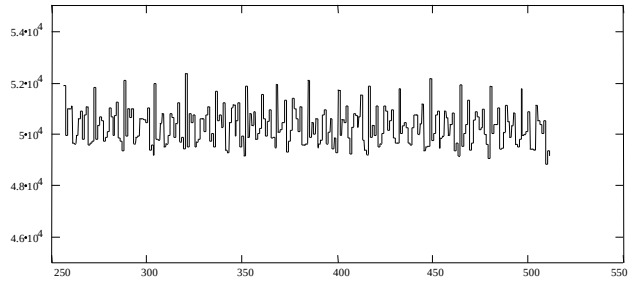

Figure 2a. The raw random time spectrum, without the sliding scale. Note the suppressed zero on the vertical axis. The peak to peak deviation is 7%, and displays the repetitive DNL of the interpolator.

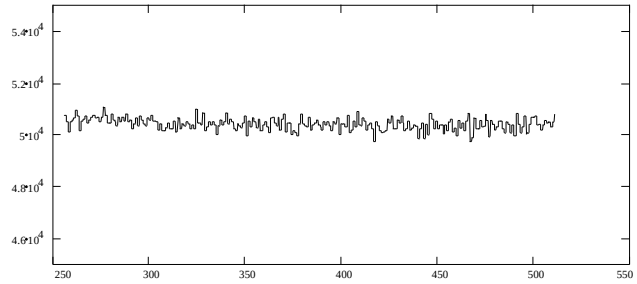

Figure 2b. The random time spectrum with the sliding scale. Note the suppressed zero on the vertical axis. The measured rms deviation is 0.46%. The expected rms deviation is 0.44% (sqrt(n)/n).

The two spectra were recorded simultaneously to eliminate any possible time dependent behavior. Note the suppressed zero on the Y axis. The expected deviation is 0.44% (rms) based on the approximately 50,000 events in each histogram element.

Figure 3a and 3b are the results of a fourier analysis of the data in Figures 2a and 2b. Note that the scales on the Y axis are *not* equal. Without the sliding scale, there are substantial amplitudes at periods of 8, 4 and 2, corresponding to250 MHz, 500 MHz and 1 GHz. Smaller peaks are found at the 3rd harmonic of 250 MHz, and oddly, the 5th and 7th harmonic of 125 MHz (no 125 MHz peak). With the sliding scale, all of these peaks are suppressed to undetectable levels.

The variable delay was between the pulse generator and the common input of the 3377. The delay varied between 0 and 3.5 nS, in 0.5 nS steps, This range (just 8 steps) is sufficient to completely remove the interpolator DNL. Tests using a wider sliding scale range (up to 31.5 nS) gave a similar result.

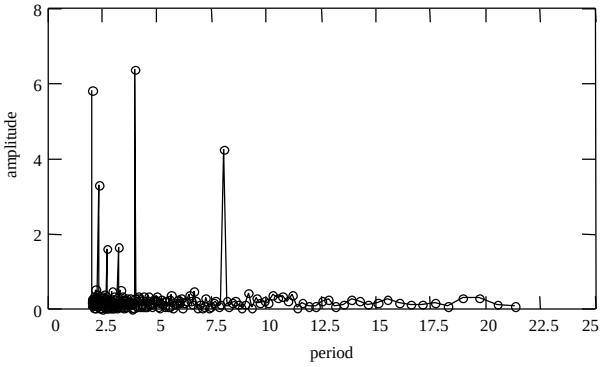

Figure 3a. Fourier amplitudes vs period of the data in Figue 2a, without the sliding scale. A period of 8 corresponds to the clock frequency, 250 MHz.

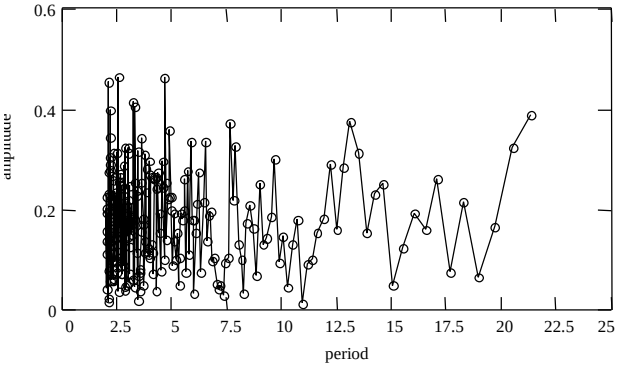

Figure 3b. Fourier amplitudes of the data in Figure 2b, with the sliding scale. Note that the vertical scale is *not* the same as Figure 2a.

A random time spectrum is easy to understand, but rather dull. If everything works properly, the spectrum is flat. A more interesting example is to measure a gamma ray spectrum with the tdc. To convert the pmt amplitude to a time difference we used a comparator to produce a signal whose width was equal to the time over threshold of the signal. If the decay of the signal is long compared to the rise time and is an exponential decay (true for NaI), this width is proportional to the log of the amplitude. This comparator signal was differentiated with a LeCroy 2366 and a fixed twisted pair delay line, to produce two pulses, one at the leading edge of the comparator signal and one at the trailing edge. The 2366 also produced a delayed pulse to use as the common stop for the 3377. The width spectrum was measured by measuring the time separation between the leading and trailing edge pulses. The variable delay was inserted between the leading edge pulse and the 3377 input. Note that if the variable delay was in the common stop (as in the random measurement), the sliding scale would have no effect. The sliding scale must affect the time difference actually being measured, in this case the difference between the leading edge pulse and the trailing edge pulse. Figure 4 shows a portion of the Na^{22} spectrum, with and without the sliding scale. The very obvious DNL in figure 4a (without the sliding scale) is completely absent in figure 4b (with the sliding scale).

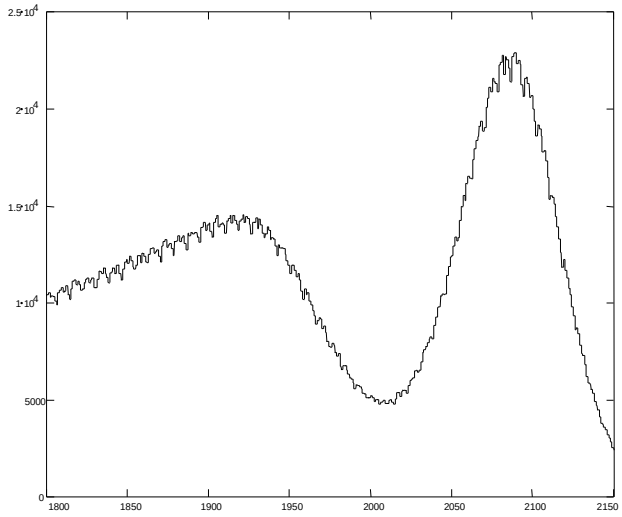

Figure 4a. Part of a Na^{22} spectrum, without the sliding scale.

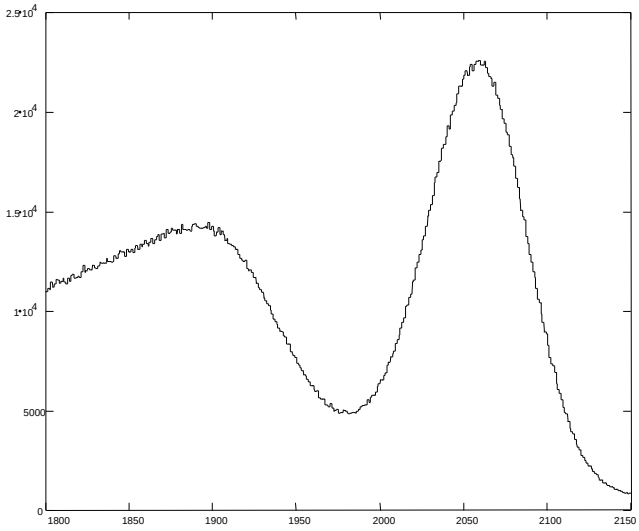

Figure 4b. The same part of a Na^{22} spectrum, with the sliding scale. The repetitive DNL produced by the interpolator is completely eliminated.

V. SUMMARY

This study was begun to determine the origin of the small (about 1% p-p) residual DNL measured in the first production modules of the CMC080 ADC [5]. The MTD133b is used in this ADC to measure the rundown times of the charge to time converter. The module incorporates a delay line sliding scale to reduce the DNL from the TDC chip. The residual DNL in the CMC080 is quite different in character (nearly all 250 MHz, some 3rd harmonic) from the DNL observed here. We conclude that the residual DNL is produced in the charge to time converter by interference from the tdc clock, and not produced in the tdc.

The delay line sliding scale is a simple technique that can easily be added to many time measurements. It is useful in any application that is sensitive to DNL. Although the MTD133b was studied here, the sliding scale method can be used with any tdc chip that exhibits similar DNL.

VI. REFERENCES

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