FASTCAMAC DRAFT SPECIFICATION VERSION 1.13

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FASTCAMAC is an extension of the CAMAC standard. The FASTCAMAC specification is organized in two levels. Level 1 is the simplest form of FASTCAMAC and the easiest to implement. It increases the maximum data transfer rate from 3 Megabytes per second to 7.5 Megabytes per second. Level 2 requires tri-state drivers, and provides transfer rates as high as 30 Megabytes per second. An option to either Level 1 or Level 2 combines the CAMAC R and W lines into one 48 bit bi-directional bus, to double the maximum transfer rate to 60 Megabytes per second (Level 2). FASTCAMAC also defines an optional multiple module block transfer. FASTCAMAC is compatible with the existing CAMAC standard. This is the specification (with minor corrections) submitted to the NIM committee, for inclusion in the CAMAC standard. This specification is to be used for the design of FASTCAMAC modules and controllers.

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The most recent specification can be found at http://www.yale.edu/fastcamac

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FASTCAMAC PROTOCOL OUTLINE FOR CAMAC MODULES

COMPATIBILITY with STANDARD CAMAC

MANDATORY

All module functions MUST be accessible via normal CAMAC on power up. The module MUST be completely functional as a normal CAMAC module. FASTCAMAC functions must be accessed by separate commands. The FASTCAMAC functions must not share Function codes and subaddresses with normal CAMAC commands.

BASIC LEVEL 1

MANDATORY

- All signals on the dataway must meet the normal CAMAC electrical requirements.
- Use normal CAMAC cycle timing until S1.
- The FASTCAMAC cycle contains multiple S1 pulses with 200 ns width and 200 ns spacing.
- The controller latches the data on the 24 R lines at the same time that it asserts S1. Data is transferred on the first S1 leading edge. The module asserts the next data word shortly after the leading edge of S1 is received.
- Use normal CAMAC cycle timing after the last S1.
- The data transfer is at a fixed rate, with a transfer every 400 ns.
- Use open collector dataway drivers, the same as normal CAMAC.
- Use the reserved read function code F(5) to indicate a FASTCAMAC basic Level 1 read operation.

OPTIONAL

- The FASTCAMAC module should (STRONGLY RECOMMENDED) protect itself against noise produced on the N, F and A lines due to possible ground bounce and crosstalk when the module changes the data on the dataway. A suggested method is to latch the N, F and A lines at the leading edge of the first S1. The latches are returned to transparent mode at the end of the FASTCAMAC cycle (signaled by S2). If BUSY is used by the module, it should also be protected.
- The S1 and S2 control pulses should (STRONGLY RECOMMENDED) also be protected against possible noise produced when the data changes on the dataway. A suggested method is to disable detection of changes in S1 or S2 during the short period when the module is changing the data on the R lines. The correct timing for this protection is known only to the module designer, and cannot be specified here. For the open collector drivers used in normal CAMAC, the protection should extend for at least 30 ns after the new data is asserted. This is sufficiently long to cover most of the ringing and ground bounce, which occurs on a transition from logic 0 to logic 1.

A module which, implements all of the mandatory items above (including the compatibility requirement), can be said to conform to FASTCAMAC basic Level 1. The maximum data transfer rate for basic Level 1 is 7.5 megabytes per second.

BASIC LEVEL 2

MANDATORY

- Tri-state (or equivalent) drivers are required for the R lines and the Q line (these drivers are used only for FASTCAMAC, the module MUST use open collector drivers for normal CAMAC commands, in compliance with the CAMAC standard).
- Level 2 uses multiple S1 pulses with programmable speed, as fast as 100 ns width and 100 ns spacing. Either the leading edge only, as in level 1, or both the leading edge and the trailing edge of the S1 pulses can be used as a data strobe. During dual edge transfers, both the module and the controller must be prepared to deal with a possible extra S1 edge, which may occur at the end of the transfer. The controller must complete the last S1 pulse, and the module must ignore the extra (last) edge. The spacing between the last S1 pulse and the S2 pulse must be at least as long as the space between S1 pulses.
- The leading edge of the first S1 pulse is not used to transfer data in a read command. This behavior is MANDATORY. The first S1 edge on a Level 2 FASTCAMAC read operation does not actually transfer valid data, rather it enables the tri-state drivers and begins to drive the dataway with the first data word. The controller will actually store the first data word on the next S1 data strobe (the leading edge of the second S1 pulse for single edge transfers or the trailing edge of the first S1 pulse for dual edge transfers). The dataway drivers should be returned to open collector mode at the leading edge of S2.
- The FASTCAMAC module must (MANDATORY) protect itself against noise produced on the N, F and A lines due to possible ground bounce and crosstalk when the module changes the data on the dataway. This is much more severe when using typical tri-state drivers than with open collector drivers. A suggested method is to latch the N, F and A lines at the leading edge of the first S1. The latches are returned to transparent mode at the end of the FASTCAMAC cycle (signaled by S2). If BUSY is used by the module, it must also be protected.
- The S1 and S2 control pulses must (MANDATORY) also be protected against possible noise produced when the data changes on the dataway. A suggested method is to disable detection of changes in S1 or S2 during the short period when the module is changing the data on the R lines. The correct timing for this protection is known only to the module designer, and cannot be specified here. The protection should extend for at least 30 ns after the new data is asserted, or for 80 ns after the S1 edge, whichever is longer. This is sufficiently long to cover most of the ringing and ground bounce (which occurs on all data transitions in Level 2).
- A control register (described in the section FASTCAMAC Control Register and Parameter P format) is required in all modules implementing FASTCAMAC level 2.
- Any FASTCAMAC Level 2 module must be capable of functioning correctly as a FASTCAMAC basic Level 1 module.

A module which, implements all of the items above (including the compatibility requirement and Level 1), can be said to conform to FASTCAMAC basic Level 2. The maximum data transfer rate for basic Level 2 is 30 Megabytes per second.

OPTIONAL FEATURES FOR LEVEL 1 AND LEVEL 2

Any FASTCAMAC module that implements an optional feature (described below) must also be able to operate as a basic FASTCAMAC module.

WRITE COMMANDS

This protocol can be optionally added to either FASTCAMAC basic level 1 or level 2.

- FASTCAMAC write commands are optional for both level 1 and level 2. Not all FASTCAMAC modules will require high-speed write capability.
- In contrast to the read commands, write commands always transfer data on the first S1 data strobe. Both single and dual edge modes are allowed. The dual edge mode can transfer an even number of words only.
- The Q response signals that the transfer was successful. Q stop modes are allowed (to signal a buffer full condition, for example). The controller and host must be prepared to count the number of successful transfers.

WIDE DATA TRANSFERS

This protocol can be optionally added to either FASTCAMAC basic level 1 or level 2.

- For wide data transfers, use both the 24 read lines and the 24 write lines as a 48 bit bi-directional dataway for read and write transfers.
- Wide data word widths of 32 bits (R1-16 and W1-16) and 48 bits are permitted. The bit mapping is different for read and write transfers.
- During read commands, the lsb is always R1. For wide 32 bit reads, the 16^{th} bit is R16, the 17^{th} bit is W1, and bit 32 is W16. For wide 48 bit reads, the 24^{th} bit is R24, the 25^{th} bit is W1 and bit 48 is W24.
- During write commands, the lsb is always W1. For wide 32 bit writes, the 16^{th} bit is W16, the 17^{th} bit is R1, and bit 32 is R16. For wide 48 bit writes, the 24^{th} bit is W24, the 25^{th} bit is R1 and bit 48 is R24.
- Wide write operations require receivers on the dataway write lines. These receivers must be compatible with normal CAMAC, which specifies 16 ma drive capability for drivers on the R lines. Normal CAMAC expects only one or two receivers (in the controllers) on the R lines. Each module should feed less than 0.07 ma into the line, when the dataway line is in the 1 state (less than 0.5 V). This requires low input current receivers (HCT for example), normal TTL or LSTTL should not be used.
- Tri-state drivers are required for the W lines in level 2.
- During a read operation, the dataway drivers (both open collector and tri-state) for the W lines must be able to sink 48 ma (since there may be 23 receivers on each W line), in compliance with normal CAMAC.
- Noise protection for N, F, A, S1 and S2 is MANDATORY for Level 1 wide data transfers (this is already MANDATORY for Level 2).

- The maximum data transfer rate is 15 Megabytes per second for Level 1 and 60 Megabytes per second for Level 2.

MULTIPLE MODULE PROTOCOL

This protocol can be optionally added to either FASTCAMAC basic level 1 or level 2.

- Multiple modules are addressed simultaneously using a station number register in the FASTCAMAC controller. Many normal CAMAC crate controllers already implement a station number register at N(24). It is a required feature of the A-1 and A-2 crate controllers. The address N(27) (a reserved station number) is recommended for the FASTCAMAC multiple module station number register (MMR). The MMR should be written (and read, if implemented) by normal CAMAC commands to N(30), A(12), similar to the station number register. The MMR must be separate (at least logically) from the normal station number register.
- Before executing the multiple module command, the MMR must be loaded with a pattern corresponding to the participating modules and all participating modules must be loaded with their order of response in a control register in each module (MANDATORY). A FASTCAMAC command to N27 (the MMR) will execute the multiple module command. The MMR should be accessible by an auxiliary FASTCAMAC controller to allow a FASTCAMAC auxiliary controller to execute multiple module commands.
- The FASTCAMAC cycle contains multiple S1, S2 sequences.
- Each participating module should (MANDATORY for level 2) latch the N, F and A signals at the first S1 leading edge. The latch should be reset at NOT N (a filtered or deglitched N from the dataway, not the latched N). The latched function code and subaddress are the same in all modules. Obviously, different function codes or subaddresses may not be combined in a single multiple module transfer.
- Each module counts S2 pulses. There is no response by or action within module unless the S2 count matches the order of response value stored in the control register. The first module to respond has zero as its order of response. All modules must ignore S1 pulses (except for latching the F, A lines at the first S1) unless the S2 count matches the order of response.
- In level 1, the data is enabled to the dataway as soon as the S2 count matches the order or response stored in the control register. The data is removed when The S1 is accompanied by Q=0, or when the S2 count does not match. The first valid data word is stored in the controller at the first S1 edge after the S2 count matches. Since the dataway drivers are open collector, a small overlap between modules does no harm.
- In level 2, the tri-state drivers are enabled at the first S1 edge after the S2 count matches and disabled at the leading edge of the next S2 (which causes the count to no longer match). This timing specification avoids any possible tri-state overlap during the module change. The first valid data is stored in the controller at the second S1 data strobe edge, after the S2 count matches the stored order of response.
- The end of a multiple module FASTCAMAC command is signaled by NOT N. The S2 counter within each module should be reset by NOT N. If filtering or deglitching is used, the module should detect NOT N within 250 ns.

Q STOP BEHAVIOR

The data transfer rate can be increased if the last valid word in a transfer sends no Q, rather than the first invalid word (the FASTCAMAC default behavior). This can be a significant time saving for reading short variable length data blocks, and for multiple module transfers. Each module MUST provide at least one data word in this mode, so a header word may be required from each module. The FASTCAMAC control register in the module must be used to select this behavior. In the absence of a control register, the default behavior is required. This is really a system design issue, but support from the hardware is required in both the module and the controller.

FASTCAMAC TIMING SPECIFICATIONS

The CAMAC dataway lines are not terminated controlled impedance transmission lines. A typical fully loaded CAMAC dataway behaves as an unterminated transmission line with distributed capacitive loading (due to the modules in the crate). For times long compared to the length of the line (18 inches, or about 3 ns), the dataway behaves like a lumped capacitance. For a fully loaded CAMAC crate, this capacitance can be as high as 500 pF. The transition time (logic 0 to logic 1 for open collector drivers, both transitions for tri-state drivers) is determined by reflections from the ends of the line, and is typically 10 to 15 ns (for drivers which cannot drive the low Z transmission line to the final logic levels).

The timing specifications, which follow, are based on this view. Transmission line effects are ignored, and the signals are assumed to appear simultaneously everywhere on the CAMAC dataway. For a typical CAMAC crate, this is an excellent approximation.

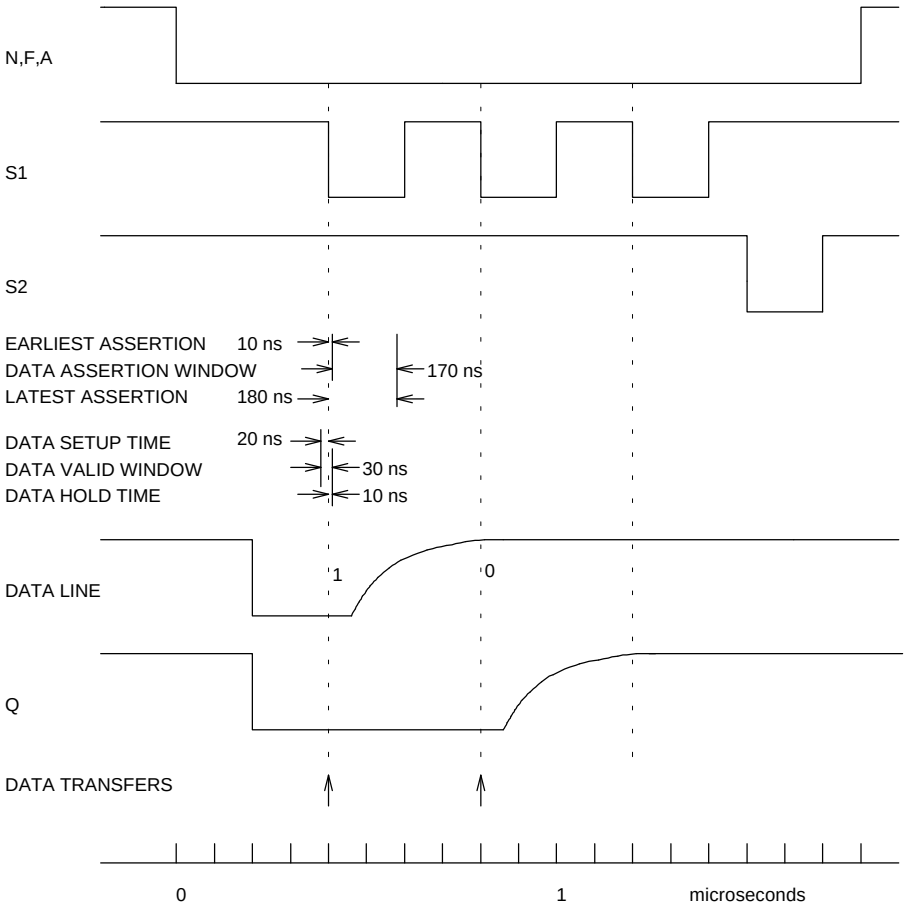
A data valid window is defined, during which a module receiving data from the dataway can be certain that the data lines are in the correct logic state. A data assertion window is also defined, during which a module is permitted to change the logic state of the data asserted on the dataway.

All data lines must be in the correct logic state at the beginning of the data valid window. The logic state of each data line must be maintained during the entire data valid window.

The data assertion window begins when the data valid window ends. The data assertion window does not include any effect due to the dataway. The module designer should use the unloaded rise and fall for the driving device to assure that the data changes occur within the data assertion window.

The time difference between the end of the data assertion window and the beginning of the data valid window represents the rise (or fall) time and the settling time on the dataway. The logic state on the dataway is permitted to change only between the end of the data assertion window and the beginning of the data valid window.

During the data valid window on the dataway, all signals must be either less than 0.8 volts or greater than 2 volts. Transitions on the dataway should be initiated only during the data assertion window.
For a transition from logic 0 to logic 1, logic 0 is detected when the voltage on the dataway drops below 0.8 Volts. For a transition from logic 1 to logic 0, logic 1 is detected when the voltage level exceeds 2 Volts.



LEVEL 1 FASTCAMAC READ BLOCK TRANSFER (2 words shown)

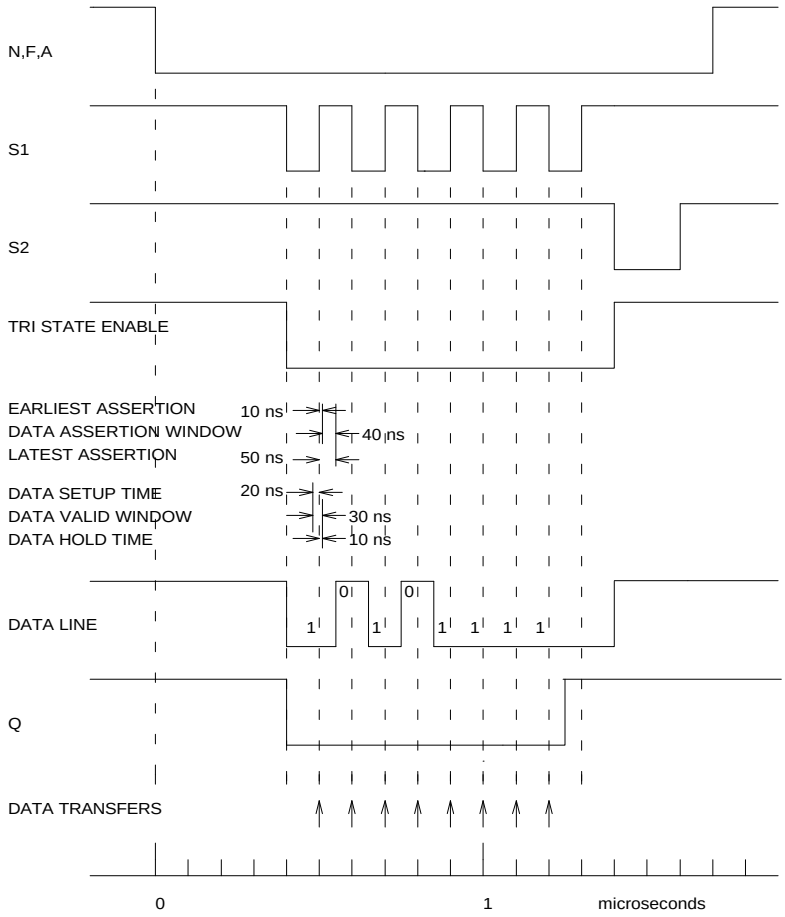
LEVEL 1 TIMING

Level 1 uses open collector drivers for the R lines and Q, the same as normal CAMAC.

The S1 pulses have a width not less than the standard CAMAC width of 200 ns and spacing equal to the width, for a minimum period of 400 ns (2.5 MHz transfer rate). The crate controller may, as an option, provide longer width and spacing if required by a particularly slow legacy module. The data will be recorded in the controller at the leading edge of S1. The first data word is transferred on the leading edge of the first S1 pulse.

The data and Q must be valid on the dataway for 20 ns before the leading edge of S1 and for 10 ns after the leading edge. This results in a data valid window on the dataway 30 ns wide

The earliest time that data can change on the dataway is 10 ns after the S1 leading edge. For a fully loaded CAMAC crate, which exhibits a 250 ns open collector time constant, the latest time should be less than 180 ns after the S1 leading edge, resulting in a data assertion window 170 ns wide.



LEVEL 2 FASTCAMAC READ BLOCK TRANSFER (dual edge, 8 words)

LEVEL 2 TIMING

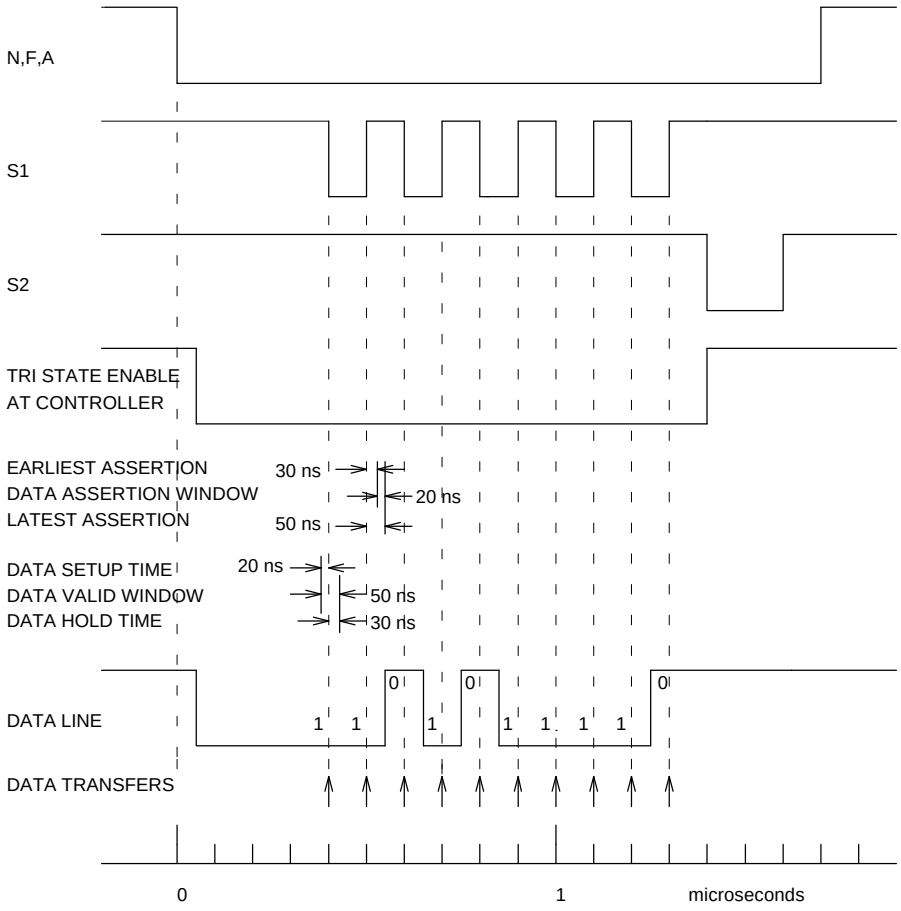
Tri-state drivers for Level 2 must be capable of driving a 500 pF load.

The tri-state drivers should be enabled at the leading edge of the first S1 pulse, and disabled at the leading edge of the S2 pulse. This timing avoids any possible tri-state conflicts on the dataway.

FASTCAMAC level 2 allows S1 width and spacing to be as short as 100 ns. Data may be transferred on the leading edge of S1 or on both edges of S1. The first data word is transferred on the second strobe, either the leading edge of the second S1 or the trailing edge of the first S1 pulse.

The FASTCAMAC level 2 S2 pulse must have the same width as a normal CAMAC S2 pulse. The S2 pulse should be separated from the S1 pulses by at least the S1 pulse spacing.

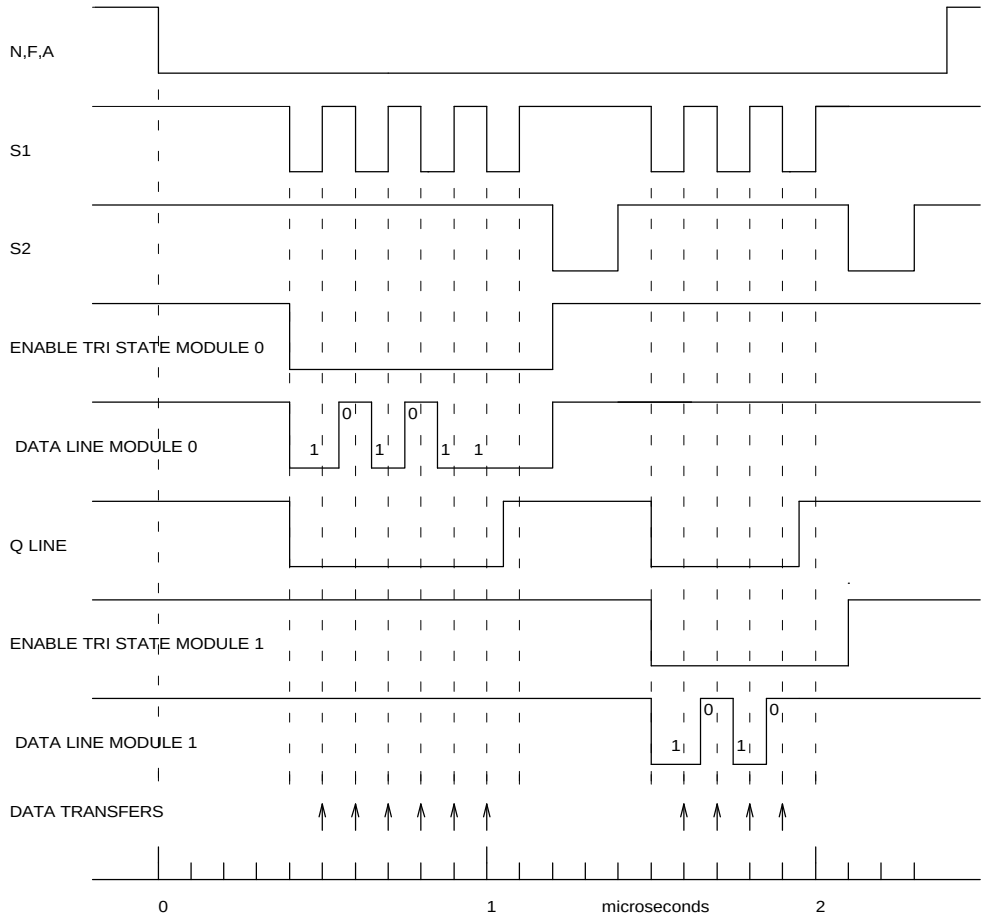
The data and Q must be valid on the dataway for 20 ns before the edge of S1 and for 10 ns after the edge, for a 30 ns data valid window. The minimum settling time on the dataway is 30 ns (for tri state drivers). The data assertion window begins 10 ns after the S1 data strobe, and ends 50 ns before the next S1 data strobe, resulting in a 40 ns data assertion window at the fastest transfer rate (100 ns period).



LEVEL 2 FASTCAMAC WRITE BLOCK TRANSFER (dual edge, 10 words)

FASTCAMAC WRITE TIMING

For a write operation, the controller must ensure that the data is valid on the dataway when the S1 strobe arrives. The controller must operate such that it provides the module with a 20 ns setup time before the S1 edge and at least 30 ns hold time (measured on the dataway). This will allow the receiving module a minimum 50ns wide data valid window. The controller must assert new data within 50 ns after the S1 edge. This allows 30 ns for settling time on the dataway (at the fastest transfer rate, 100 ns between data strobes) and results in a data assertion window only 20 ns wide. During the 20 ns data assertion window and the 30 ns settling time (from 30 to 80 ns after the S1 edge), the module should (optional for Level 1 but MANDATORY for Level 2) protect itself from possible noise due to changing the data on the dataway. Please note that this timing specification is independent of the S1 width and spacing and is different from the read operation specification. For level 2 write operations, the tri-state drivers (on the data lines) in the controller should be enabled at the start of the CAMAC cycle and return to open collector mode at the leading edge of S2.



MULTIPLE MODULE FASTCAMAC LEVEL 2 READ BLOCK TRANSFER (dual edge, 2 modules)

MULTIPLE MODULE TIMING

For a multiple module transfer, the controller produces a sequence of S1 and S2 pulses. The intermediate S2 pulses, which signal the change from module to module, have the same width as a normal CAMAC S2 pulse. The S2 pulse should be separated from the S1 pulses by at least the S1 pulse spacing. The data assertion and data valid windows are as for a single module FASTCAMAC operation.

WAIT STATES

The FASTCAMAC controller may extend the interval between S1 data strobes (either the S1 width or spacing) as required by the availability of buffer storage space (or new data in the case of write commands). This may result in larger (possibly much larger) than expected S1 width and spacing. If wait states are implemented in the controller, the controller must also implement a means of aborting a command in progress.

N-LINE TIMING

The end of a Multiple Module FASTCAMAC command is signaled by NOT N. The N line MUST be idle for at least 300 ns after a FASTCAMAC command. The module designer must ensure that NOT N is

detected within 250 ns. The N line is driven with an open collector driver, just as in normal CAMAC. This requirement precludes back to back Multiple Module commands to the same module in which the N line remains asserted between commands. For all other FASTCAMAC commands, S2 signals the end of the CAMAC cycle.

FASTCAMAC CONTROL REGISTER and PARAMETER P FORMAT

A control register is required if a FASTCAMAC module uses an optional feature. Only a basic Level 1 module for which the F5 function code, with 16 possible subaddresses, is sufficient, may do without a control register. Any module that implements Level 2, or Level 1 with any optional features, MUST have a FASTCAMAC Control Register (FCR).

There MUST be a unique FCR for each FASTCAMAC function implemented in the module. These registers affect only the FASTCAMAC behavior of the module for that function code and subaddress (or group of subaddresses that share a similar function). The capabilities of the module can be embedded in the FCR, by making the register read/write or read only, on a bit by bit basis. The host may then try to change the bits corresponding to various features, and read back the FCR to see if the feature is available for use.

A simple module implementing a single FASTCAMAC Basic Level 1 command will use a unique function code, F5, to indicate the FASTCAMAC operation. The crate controller need only recognize the F5 to change from normal CAMAC to FASTCAMAC (basic Level 1). As long as FASTCAMAC basic Level 1 read is the default meaning of F5, this is sufficient. However, for FASTCAMAC Level 2, and the optional features of Level 1, this is inadequate. The crate controller must be aware of, on a command by command basis, which FASTCAMAC features are required and which timing is to be used. The F5 command may be used for an extended level 1 (with an optional feature) or a level 2 command, as long as the default (power up) behavior of the system (module AND controller) is that F5 is a FASTCAMAC basic level 1 read command.

A parameter P is defined, that contains information to be passed to the crate controller by the software driver, in a manner similar to the way that the CAMAC module and sub-address are passed in the ESONE standard CAMAC subroutines. The actual formats of the commands to the controller are left to the controller designer. The user will see a simple software interface, the details are hidden in the driver software and in the controller. The module designer will specify the values of P allowed for each FASTCAMAC command implemented in the module, as part of the module specification.

The control register in the module (FCR), and the parameter P (to be passed to the controller) have a compatible format, described below. In the following table, Bit 1 is the least significant bit, consistent with the CAMAC numbering of the R and W signal lines. An X means that the bit is ignored. Note that the same value may be loaded in the module FCR and used as the parameter P for the controller.

FASTCAMAC Control register and Parameter P

Bits	Meaning	FCR	P
1-2	0 = normal CAMAC, 1= FASTCAMAC Level 1, 2 = level 2	✔	✔
3	0 = single edge transfers, 1 = double edge transfers	✔	✔
4	Q Response for last word, 0 = Data Invalid, 1 = Data Valid	✔	✔
5-6	Transfer width, 0 = 24, 1 = 32 (16R,16W), 2 = 48 bits (3 not used)	✔	✔
7	0 = single command, 1 = multiple module command	✔	x
8-12	Multiple module response order, 0 to 23. Bit 9 is the lsb	✔	x
13-15	S1 width and spacing, bit 13 is the lsb. 0 = 100 ns, 1 = 125 ns, 2 = 150 ns, 3 = 175 ns, 4 = 200 ns, 5 = 225 ns, 6 = 250 ns, 7 = 275 ns	x	✔
16-24	Not used	x	x

For a normal CAMAC operation, both FCR and P = 0.
For a FASTCAMAC basic Level 1 read operation, FCR = 1 and P = 4001H

LEGACY CAMAC MODULES

FASTCAMAC is compatible with normal CAMAC. Fully featured FASTCAMAC compliant modules and controllers can coexist in existing CAMAC crates with existing, normal CAMAC modules. Both can perform as intended without interference.

Many existing CAMAC module designs can be easily modified to implement some of the FASTCAMAC protocol, but may be unable to strictly comply with FASTCAMAC Basic Level 1. We expect that it may be difficult in some cases, to add extra decoding for F5, or to meet the 180 ns data assertion time requirement, without a complete redesign of the module.

For these legacy modules, exceptions to the FASTCAMAC specification are permitted, to allow a smooth transition from normal CAMAC to FASTCAMAC. For example, Level 1 operations may be assigned to other function codes than F5. By specifying operation only at the slowest S1 timing (275 ns width and spacing), the data assertion time can be extended to 330 ns after the S1 leading edge. Compatibility with normal CAMAC may be accomplished with a mechanical switch, or jumper, rather than by using separate function codes.

FASTCAMAC modules that implement Level 2, will usually be complete new designs, and are expected to be fully compliant with the FASTCAMAC specification.

CAMAC modules that are not fully compliant with the FASTCAMAC specification may not claim to be FASTCAMAC modules, but only as modules with LIMITED FASTCAMAC capability.

FASTCAMAC PROTOCOL OUTLINE FOR CAMAC CONTROLLERS

The following is a short summary of some of the requirements for a FASTCAMAC crate controller. The list is not necessarily complete, it should not be viewed as a specification for a crate controller.

- Basic Level 1 (an F(5) command), Generate multiple S1 timing, latch data at leading edge of S1.
- Basic Level 2 (an F(5) or other F command), Tri State driver for S1, Variable S1 timing (from 100 ns to 275 ns width and spacing is recommended), single or double edge transfers.
- Optional FASTCAMAC Write Transfers
- Optional FASTCAMAC Wide Transfers.
- Optional FASTCAMAC Multiple module protocol
  Must provide multiple S1, and multiple S2 sequences
  N register to address multiple modules
  The N line must become NOT N for 300 ns after a Multiple Module command.
- Optional Q-stop behavior
- Wait States. The FASTCAMAC controller must interface with the host system. In general, all data transfers will be between the FASTCAMAC module and the host system, with only limited temporary buffering in the controller. If this buffer space is full (or empty, for write commands), the controller may be unable to store (or supply) the next data word in the transfer. In this case the controller will extend the interval until the next S1 data strobe, until the data transfer can proceed. This will result in larger (possibly much larger) than expected S1 width and spacing. If wait states are implemented, a means of aborting a stalled command is required.
- Compatibility with Auxiliary Crate Controllers. The request / grant access protocol is compatible with FASTCAMAC. The ACL protocol is not compatible with the FASTCAMAC extended cycle,. FASTCAMAC controllers may generate ACL requests to gain access to the dataway, but controllers executing FASTCAMAC operations cannot respond to ACL inputs within the required access time This is very important for serial controllers, with the fixed length command and data frame.
- The end of a single FASTCAMAC command is identical to normal CAMAC. The modules may assume that S2 signals the beginning of the ending sequence. Back to back FASTCAMAC commands to the same module, in which N remains asserted between commands, are allowed, as in normal CAMAC.
- At the end of each FASTCAMAC Multiple Module Command, the controller must (MANDATORY) ensure that N becomes logic 0 for a short period for each module participating in the Multiple Module FASTCAMAC command. The period of NOT N must be at least 300 ns, to allow time for simple filtering or deglitching of the N line in the module. Immediate CAMAC commands, normal or FASTCAMAC are allowed to different modules (different N lines). If the FASTCAMAC crate controller supports an auxiliary controller, It must not relinquish control of the dataway after a FASTCAMAC Multiple Module Command until the NOT N period is completed.

A FASTCAMAC basic Level 1 command is identified to the controller by F(5). The default behavior of the controller is to treat F(5) as a FASTCAMAC basic Level 1 READ command. For FASTCAMAC level 2, and Level 1 with any optional feature, the controller must know for each command (F(5) or other), which FASTCAMAC options are implemented and the rate for generating S1 pulses. A few of the possible ways to achieve this are described below. The choice is left to the controller designer.

- A LOOK-UP TABLE. A memory array in the controller stores the parameter P for every possible F, N, A in the crate. This requires only 16k words of RAM. This RAM is loaded at system initialization. The default values are zero (normal CAMAC) except for F(5) which is FASTCAMAC basic Level 1. The F, N, & A of each command to be executed are used to form the address to this RAM to access the required parameter for that command.

- A REGISTER IN THE CONTROLLER DEDICATED PARAMETER. A single register in the controller (written with a normal CAMAC command) contains the parameter P. This could be used with all subsequent CAMAC commands, only the next command, or with the next command which uses a station number register. This method has the virtue of requiring only normal CAMAC commands to change the behavior of the controller. No changes are required to the CAMAC driver software, only to the application software. The disadvantage is that an extra normal CAMAC command is required to change modes, or to change the contents of the station number register.

- INCLUDING THE PARAMETER P WITH C, N, A, & F. In this method the parameters C, N, A, F, & P are passed by the application software to the driver, and then to the controller. For each command, FASTCAMAC or normal CAMAC, the controller has a complete description of the actions to be carried out. This method is conceptually the simplest, but does require changes to the software driver, and possibly changes to all CAMAC calls in the application programs.

EXPLANATORY NOTES

DATA ASSERTION TIME FOR FASTCAMAC LEVEL 1

The combination of the open collector drivers, pull-up resistors to +5 volts, and capacitive loading by the dataway and modules produce a rise time (logic 1 to logic 0) which is an RC time constant. This dataway time constant for a fully loaded 25-position crate has been observed to be as long as 250 ns, corresponding to a total capacitance of 500 pF (with a 500 ohm pull-up resistor). The CAMAC standard does not specify the maximum input capacitance for each module. Measurements were made on crates loaded with typical modules drawn from laboratory and university equipment stocks.

The minimum logic 0 requirement for driving the CAMAC dataway is 3.5 volts, a very conservative value. This requires 1.2 time constants, or 300 ns to rise from a logic 1 (0 Volts). The data assertion time (time from the data strobe until the new data is asserted on the dataway), must be less than 80 ns to satisfy the 20 ns setup time requirement. If we relax the minimum logic 0 requirement to 2.4 volts (the value prescribed by the CAMAC standard for external signals), only 0.65 time constants are required, or 163 ns. This allows the data assertion time to be as long as 217 ns. We recognize that an assertion time of 80 ns may be difficult to achieve with inexpensive circuits, and that 2.4 volts represents a substantial reduction in noise immunity from the standard CAMAC value of 3.5 volts. The specification of 180 ns for the end of the data assertion window allows 200 ns for signal rise on the dataway, which corresponds to 2.9 volts for the minimum logic 0, a reasonable compromise.

TRI-STATE DRIVERS

In normal CAMAC, the use of tri-state drivers affects only the ability to OR data from multiple modules on to the dataway. The transitions and noise due to changing the data on the dataway occur at the

beginning of the cycle, while the S1 and S2 lines are at logic 0 (pulled up to +5V), and are least susceptible to noise on the dataway. Since the dataway also idles with the data lines at logic 0, the slow 'rise' time (logic 1 to logic 0) of the open collector drivers is not relevant. Only the fall time (logic 0 to logic 1), which is a fast transition (10-20 ns) even with open collector drivers, affects the ability of a module to place valid data on the dataway by S1.

FASTCAMAC level 2 requires tri-state drivers, since the slow logic 1 to logic 0 transition with standard open collector drivers affects the ability to change the data between S1 data strobes and precludes data transfers faster than 400 ns.

It is possible to use a complex PLD as a dataway driver to allow dynamic selection of open collector or tri-state with a single driver. A complex PLD can also provide a bi-directional transceiver function. The PLD must have individual control of output enables. For wide transfers, the drivers on the W lines must be capable of sinking 48 ma.

PROTECTION FROM DATAWAY NOISE FOR N, F, A, S1 and S2

When new data is asserted by a module, it can produce ground bounce which affects the control lines (N, F, A, S1, S2, etc) entering the module. The amplitude depends on the net number of lines switching in the same direction and the inductance of the ground connection to the module. The ground bounce usually decays within 20 to 30 ns. This is not seen by other modules, or by the controller, but it can cause a transient error in the decoding of the control lines by the module driving the data lines. This problem occurs in normal CAMAC with open collector drivers when the data is predominately logic 1. The ground bounce when the drivers are initially asserted (before S1) can cause one of the asserted N, F or A lines to appear as logic 0, causing the drivers to be turned off. This can produce an oscillation, and is often seen when CAMAC modules are operated on an extender board. This is typically cured by filtering the buffered N, F and A lines with a simple RC time constant of 50 to 100 ns. This effect can be minimized by making the inductance of the ground connection as low as possible. The CAMAC specification allows the two ground fingers to be extended to the edge of the board, and this should always be done.

In FASTCAMAC the problem can also occur shortly after each S1 edge, when the data changes on the dataway. With the tri-state drivers the problem can occur on both rising and falling data transitions. The effect is largest for wide transfers in which all 48 bits switch in the same direction. For FASTCAMAC Level 2 and wide Level 1 transfers, simple filtering is not sufficient, and the N, A and F lines should be latched at the first S1 leading edge, and not released until the end of the command.

The S1 and S2 signals obviously cannot be latched, and sufficient filtering on S1 would substantially reduce the maximum transfer rate. For FASTCAMAC read commands, disabling the detection of an edge for 30 ns after the data change is initiated on the dataway will protect S1. Since the module is initiating the data change, this timing is entirely within the control of the module designer.

A simple method to accomplish this is to use an RS flip flop and provide a delayed copy of S1 (S1D). The detection of the leading edge of S1 (set the flip flop) is enabled only when S1D is false. The detection of the trailing edge (reset the flip flop) is enabled only when S1D is true. The delay should be less than the width of the S1 pulse and longer than the noise on the dataway (30 ns after the data change).

For maximum protection, it may be desirable to provide a different delay for level 1 and level 2, perhaps 180 ns for level 1 and 80 ns for level 2 (for 100 ns S1 pulses).

During a write command, ground bounce is not a serious problem for the receiving module (because the controller asserts the data). However, the controller must assert the new data within 50 ns after the S1 edge. This allows the module to protect itself from dataway noise by disabling edge detection for 80 ns after the S1 edge.

S2 should also be protected, either similar to S1, or by sufficient filtering (50 to 100 ns RC).

Note that some form of protection is MANDATORY for Level 2. It is optional for Level 1 except for wide transfers, where it is also MANDATORY.

PIPELINE REGISTER

In FASTCAMAC level 2, a pipeline register can be utilized to shorten the data assertion time on the dataway. The tri-state drivers are enabled at the leading edge of the first S1 pulse. If the first data word is latched in a pipeline register at this time, the module can begin to fetch the second word (incrementing the address, etc.). The actual data access time within the module is then separated from the dataway by this pipeline stage. The data assertion delay on the dataway can be quite short, just the latch propagation delay and the driver propagation delay.

N LINE

The FASTCAMAC protocol (Level 2) latches the CAMAC control lines (N, F, & A) to provide immunity from the noise produced by the changing data lines. For single FASTCAMAC commands, these latches can be released when S2 is detected. For Multiple Module FASTCAMAC commands these latches are released when NOT N is detected (since the FASTCAMAC multiple module protocol produces a sequence of multiple S1s and S2s, S2 is not a valid indicator of the end of the FASTCAMAC command). A side effect of this behavior is that the FASTCAMAC controller MUST remove N for a short period at the end of each FASTCAMAC Multiple Module command. This precludes back to back Multiple Module commands to the same module in which the N line remain asserted between commands (this is an allowed behavior for normal CAMAC, and single FASTCAMAC commands).